Referring to FIG. **26**A, an electrode layer **116** is formed on a substrate **105**. The substrate **105** may include, for example, a silicon substrate, a silicon carbide (SiC) substrate, or an aluminum oxide (for example, Al2O3) substrate, but example embodiments are not limited thereto. The electrode layer **116** may include a metal or a metal nitride. As illustrated in FIG. **26**B, the electrode layer **116** is patterned into source **110**, gate **112**, and drain **114** electrodes. As illustrated in FIG. **26**C, a depletion film **104'** is formed over the source electrode **110**, gate electrode **112**, and drain **114** electrodes. The depletion film **104'** may contain the same material as the depletion layer **50** described above with reference to FIG. **4**, but example embodiments are not limited thereto.

Next, as illustrated in FIG. **26**D, a depletion layer **104** is formed by etching back the depletion film **104'** formed over the source **110**, gate **112**, and drain **114** electrodes. As illustrated in FIG. **26**E, a first channel supply film **103'** is formed over the depletion layer. The first channel supply film **103'** may contain the same the material as the first channel supply layer **36** described above with reference to FIG. **4**, but example embodiments are not limited thereto. As illustrated in FIG. **26**F, a first channel supply layer **103** is formed by etching back the first channel supply film **103'**. The first channel supply layer **103** may partially expose the depletion layer **104**. Next, as illustrated in FIG. **26**G, a channel layer **102** and a passivation layer **101** are sequentially formed over the first channel supply layer **103**. The channel layer **102** may contain the same material as the channel layer **34** described above with reference to FIG. **4**, but example embodiments are not limited thereto. The passivation layer may contain an insulating material, such as an oxide (e.g., silicon oxide) or an insulating polymer material, but example embodiments are not limited thereto.

While FIGS. **26**A to **26**G illustrate a method according to example embodiments of forming a HEMT that includes a depletion layer **104**, one having ordinary skill in the art would appreciate that a depletion layer **107** may be formed on a second channel supply layer **106** (as shown in FIG. **25**B) instead of forming the depletion layer **104**. Referring to FIG. **25**B, the second channel supply layer **106** and the depletion layer **107** may include the same materials as the second channel supply layer **38** and depletion layer **40**, respectively, as described above with reference with FIG. **1**.

While some example embodiments have been particularly shown and described, it will be understood by one of ordinary skill in the art that variations in form and detail may be made therein without departing from the spirit and scope of the claims. Descriptions of features or aspects of some HEMTs according to example embodiments should typically be considered as available for other similar features or aspects in other HEMTs according example embodiments.

What is claimed is:

1. A high electron mobility transistor, comprising:
- a substrate;
- a channel layer on the substrate,
  - the channel layer being a GaN layer,
  - the channel layer including a 2DEG channel and a depletion area;
- a first channel supply layer on the channel layer and corresponding to the 2DEG channel,
  - the first channel supply layer defining an opening that exposes the depletion area;
- a depletion layer on the first channel supply layer and on the depletion area;
- a second channel supply layer between the depletion layer and the depletion area,
  - the second channel supply layer including a portion that is on an upper surface of the first channel supply layer and extends over the 2DEG channel,
  - an aluminum (Al) content of the second channel supply layer being different from an aluminum (Al) content of the first channel supply layer,
  - a polarizability of the second channel supply layer being less than a polarizability of the first channel supply layer, and
  - the first and second channel supply layers both including an aluminum compound;
- source and drain electrodes spaced apart on the first channel supply layer; and
- a gate electrode on the depletion layer, wherein
- the depletion layer is not directly in contact with the first channel supply layer, and
- the depletion layer is configured to remove a 2DEG that is generated in the depletion area of the channel layer by the second channel supply layer.

2. The transistor of claim **1**, wherein the depletion layer contacts at least one of the source and drain electrodes.

3. The transistor of claim **1**, further comprising:
- an insulation layer between the gate electrode and the depletion layer.

4. The transistor of claim **1**, wherein
- a polarizability of the depletion layer is less than a polarizability of the first channel supply layer,
- the depletion layer includes a compound semiconductor layer doped with a p-type dopant.

5. The transistor of claim **1**, wherein
- a polarizability of the depletion layer is less than a polarizability of the first channel supply layer and
- a concentration of a polarization generation component in the depletion layer varies according to a thickness of the depletion layer.

6. The transistor of claim **1**, wherein
- the first channel supply layer contains an n-type dopant, and
- the first channel supply layer comprises at least one of aluminum (Al), gallium (Ga), and indium (In).

7. The transistor of claim **1**, wherein a thickness of the first channel supply layer is about 20 nm to about 200 nm.

8. The transistor of claim **1**, wherein
- a polarizability of the second channel supply layer is less than a polarizability of the first channel supply layer.

9. The transistor of claim **8**, wherein
- the depletion layer includes at least one of aluminum (Al), gallium (Ga), and indium (In).

10. The transistor of claim **8**, wherein
- the first and second channel supply layer are compound semiconductor layers having the same elements but different composition ratios.

11. The transistor of claim **8**, wherein
- a thickness of the first channel supply layer is about 20 nm to about 200 nm and,
- a thickness of the second channel supply layer is about 5 nm to about 20 nm.

12. The transistor of claim **1**, wherein the gate electrode includes at least one a metal and a nitride.

13. The transistor of claim **1**, wherein the second channel supply layer includes at least one of:
- a lower pair of sidewalls that extend perpendicular from the channel layer and are between a corresponding pair sidewalls in the first channel supply layer; and
- an upper pair sidewalls that extend perpendicular from the first channel supply layer and contact the source and drain electrodes, respectively.